

FROM

(WED) DEC 10 2003 12:22/ST. 12:21/NO. 6329645707 P 8

IN RE: APPLICATION S.N. 09/740,751
JIANG ET AL.
RESPONSE TO DECEMBER 10, 2002 OFFICE ACTION

Pursuant to 37 C.F.R. § 1.121, "marked up" versions of the foregoing amendments, highlighting the amendments made, appear on the "separate sheets" comprising Appendix A to this Response.

REMARKS

1. *Status of the Application.* Claims 18-19, 21-23, 26, 27, 29-32, 34-36, 39, 40, and 42-46 are pending in the application. Claims 18 and 31 are amended herein; no new matter is added by way of these amendments.
2. *The Section 112 Rejections.* Claims 18-19, 21-23, 26, 27, 29-32, 34-36, 39, 40, and 42-46 were rejected under 35 U.S.C. § 112, first and second paragraph, with the Office Action alleging that the claims do not sufficiently specify and ordering to the recited method steps. Although Assignee believes that the claims, interpreted in light of the Specification, were abundantly clear as to the ordering of the method steps, Assignee has amended the claims herein to include an explicit indication of ordinance ("first," "second," "third," etc..) to each recited method step. After entry of these amendments, there can be absolutely no question as to the order in which the method steps must be performed. Reconsideration of the § 112 rejection on this basis is therefore respectfully requested.

With respect to claim 29, the Office Action inquires "what is a spin-on process[?]" and "what is [sic] photo define/etch process got to do with the claims[?]" Assignee respectfully but strenuously contends that these inquiries were fully addressed in the Assignee's previous Response to September 25, 2002 Office Action, and the portion of that Response addressing these inquiries are hereby incorporated by reference in to this Response.

Summarizing Assignee's position with regard to the notoriety of spin-on semiconductor processing, Assignee has proffered ample and irrefutable evidence that the term "spin-on" is widely used in the semiconductor industry, and would be instantly recognized and unambiguously understood by any person of ordinary skill in the semiconductor arts. Assignee

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has presented a representative sampling of the thousands of issued U.S. patents which use the term "spin-on" in their claims.

As further evidence of the widespread and common use and understanding of spin-on processes and techniques, accompanying this response is a copy of U.S. Patent No. 6,530,340 to You et al., entitled "Apparatus for Manufacturing Planar Spin-on Films." In a "Discussion of the Related Art," the '340 patent states matter-of-factly that "Spin-on deposition methods are used for the manufacture of thin films on semiconductor devices." ('340 patent, col. 1, lines 49-50). The '340 patent goes on to discuss perceived "problems" with "conventional" and "typical" spin-on methods." ('340 patent, col. 1, line 59 through col. 2, line 63). It is submitted that the '340 patent provides more than ample support for the premise that spin-on processing, and the term "spin-on" are well-known to persons of ordinary skill in the art, such that the use of that term in the claims of the present application cannot provide the basis for a § 112 rejection.

It is further respectfully submitted that the suggestion that claim 29 must recite the "required steps of spin on process [sic]" is improper. Claim 29 merely clarifies that the process of forming the first layer, as recited in claim 18, can be accomplished with spin-on processing, as opposed to some other suitable manner. Being a well-known semiconductor processing technique, there is no basis for requiring the claim to specifically recite the "required steps of spin-on process."

With regard to Office Action's inquiry as to the meaning of the term "define/etch," claim 29 has been amended to clarify the meaning that would be understood by persons of ordinary skill in the art, *define and etch*.

The Office Action states that "[i]t sounds like the photo define/etching process removes rather than bonding the first material," and that "[t]his process contradicts the bonding process as recited in the claims." It is respectfully submitted that the meaning of claim 29 would be completely and unambiguously clear to any person of ordinary skill in the art. It is common knowledge that formation of semiconductor structures on a substrate can be accomplished by forming a thin film of a desired material over an area larger than the size of a device to be formed (in many cases, the entire substrate), and then etching away selected portions of the film to leave

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only the desired structure remaining. Formation of the thin film can be accomplished in various ways, including chemical vapor deposition and spin-on processes, while the etching away can be accomplished through a photo-define and etch process. The "define" portion involves specifying what areas of the thin film are to be removed and what areas are to remain, and the "etch" portion involves removing the areas specified to be removed. It is submitted that claim 29, as amended herein, would be entirely unambiguous to persons of ordinary skill in the art.

4. *The Section 103 Rejections.* Claims 18-19, 21-23, and 26-27 were variously rejected under 35 U.S.C. § 103 as being unpatentable over certain hypothetical combinations of prior art references, including U.S. Patent No. 4,513,055 to Leibowitz ("Leibowitz"), U.S. Patent No. 6,274,932 to Mikagi ("Mikagi"), and U.S. Patent No. 6,187,700 to Merkel ("Merkel"). As discussed below, it is respectfully submitted that these rejections are improper and not supported by the prior art cited.

Each of the § 103 rejections in the Office Action were made in the last Office Action issued on September 25, 2002, and each of these rejections was responded to in Assignee's Response to September 25, 2002 Office Action submitted on October 4, 2002. Assignee's responses to the rejections in the October 4, 2002 Response are hereby incorporated by reference herein.

Summarizing Assignee's responses, it is respectfully submitted that the Office Action wholly fails to make out the *prima facie* case of obviousness that it must.

A rejection based on §103(a) must establish three basic criteria in order to establish a *prima facie* case of obviousness. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to modify the reference or combined referenced teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP §§706.02(j); *see also* 2142. Specifically, since "invention itself is the process of combining prior art in a non-obvious manner," to establish

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obviousness the "Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed." *In re Rouffet*, 47 USPQ2d 1453, 1458 (Fed. Cir. 1998). Importantly, examiners are forbidden from "the use of hind-sight in the selection of references that comprise the case of obviousness." *Id.*

As with all rejections, the burden is on the Examiner to establish an "unrebutted *prima facie* case of obviousness." *Id.* at 1455. "An applicant may specifically challenge an obviousness rejection by showing that the [Examiner] reached an incorrect conclusion of obviousness or that the [Examiner] based its obviousness determination on incorrect factual predicates." *Id.* As discussed below, it is respectfully submitted that the Office Action does not present a *prima facie* case of obviousness as to the present rejections, in that it fails to make a *prima facie* showing that persons skilled in the art would have made the proposed hypothetical combination, and further that it fails to make a *prima facie* showing that the proposed combination, if made, would achieve the objectives of the present invention.

The ultimate determination of whether an invention is or is not obvious is a legal conclusion based on underlying factual inquiries including: (1) the scope and content of the prior art; (2) the level of ordinary skill in the prior art; (3) the differences between the claimed invention and the prior art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18; 148 USPQ 459, 467 (1966).

"[W]hen the issue is obviousness, 'it is fundamental that rejections under 35 U.S.C. §103 must be based on evidence comprehended by the language of that section.' *In re Grasselli*, 713 F.2d 731, 739, 218 USPQ2d 769, 775 (Fed. Cir. 1983). The essential factual evidence on the issue of obviousness is set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966) and extensive ensuing precedent. The patent examination process centers on prior art and analysis thereof. When patentability turns on the question of obviousness, the search for and analysis of the prior art includes evidence relevant to the finding of whether there is a teaching, motivation, or suggestion to select and combine the references relied on as evidence of obviousness. See, e.g., *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351-52, 60 USPQ2d 1001, 1008 (Fed. Cir. 2001) ("the central question is whether there is reason to combine [the] references," a question of fact drawing on the *Graham* factors).

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'The factual inquiry whether to combine references must be thorough and searching.' *Id.* It must be based on objective evidence of record. This precedent has been reinforced in myriad decisions, and cannot be dispensed with. *See, e.g., Brown & Williamson Tobacco Corp. v. Philip Morris Inc.*, 229 F.3d 1120, 1124-25, 56 USPQ2d 1456, 1459 (Fed. Cir. 2000) ("a showing of a suggestion, teaching, or motivation to combine the prior art references is an 'essential component of an obviousness holding' ") (quoting *C.R. Bard, Inc. v. M3 Systems, Inc.*, 157 F.3d 1340, 1352, 48 USPQ2d 1225, 1232 (Fed. Cir. 1998)); *In re Dembiczaik*, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999) ("Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references."); *In re Dance*, 160 F.3d 1339, 1343, 48 USPQ2d 1635, 1637 (Fed. Cir. 1998) (there must be some motivation, suggestion, or teaching of the desirability of making the specific combination that was made by the applicant); *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988) ("teachings of references can be combined *only* if there is some suggestion or incentive to do so.") (emphasis in original) (quoting *ACS Hosp. Sys., Inc. v. Montefiore Hosp.*, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984)).

The need for specificity pervades this authority. *See, e.g., In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); *In re Rouffet*, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggest the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); *In re Fitch*, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references."). *In re Lee*, 61 USPQ2d 1430, 1433-34, (CAFC 2002).

In the present application, the subject matter of claimed invention taken as a whole would have been unobvious to a person skilled in the art at the time of the invention. There is no suggestion or incentive to combine the cited art to achieve Applicant's claimed invention. The Office Action has not provided any particular finding as to the reason a skilled artisan, with no

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knowledge of the claimed invention, would have selected components for combination in the manner claimed. *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000), cited in *In re Lee*, 61 USPQ2d 1430 (CAFC 2002).

First and foremost, it is noted that *Leibowitz* is directed to a *printed circuit board*, and makes no mention whatsoever of the subject matter of the present application, namely electrical contact sockets. *Leibowitz* appears to be concerned with providing a composite printed circuit board having a coefficient of thermal expansion that be "regulated or adjusted to closely match the thermal coefficient of chip carriers by varying ... the ratio of volumes (and hence weights) of the positive and negative thermal coefficient yarns of the thermal coefficient control fabric." *Leibowitz*, col. 3, lines 38-43.

Likewise, *Mikagi* is directed to subject matter wholly unrelated to the subject matter of the present application. *Mikagi* appears to be directed to a multilevel interconnection structure in a semiconductor device, and like *Leibowitz* makes no reference whatsoever to contact pin sockets for packaged semiconductor devices.

The "aperture" alleged by the Office Action to be shown in *Mikagi* is not a socket, but an "interlayer contact hole" reaching the diffusion layer of a semiconductor substrate. See, *Mikagi*, col. 6, line 41-44. From Figures 2D and 2E in *Mikagi* and associated portions of the *Mikagi* specification, it is clear that this interlayer contact hole is ultimately filled with an aluminum film 114 (see, *Mikagi*, col. 2, lines 7-9). Thus, *Mikagi*, like *Leibowitz*, wholly fails to teach or suggest formation of a "contact."

From the foregoing discussion, it is apparent that (1) the Office Action provides no basis for concluding that a person of ordinary skill in the art would be motivated in any way to make the proposed hypothetical combination of *Leibowitz* and *Mikagi*; and (2) that even if the proposed hypothetical combination was made, this would not even remotely achieve the objectives of the present invention, given that neither *Leibowitz* nor *Mikagi* relates in any way to the subject of contact pin sockets and their formation. Reconsideration and withdrawal of the § 103 rejections of claims 18-19, 21, and 26 is therefore requested.

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Claims 22, 23, and 27 were rejected under § 103 as being unpatentable over the proposed hypothetical combination of *Leibowitz* and *Mikagi* as applied to the claims discussed above, further in view of *Merkel*. It is submitted that the foregoing discussion of the *Leibowitz/Mikagi* combination is equally applicable to the rejection of claims 22, 23, and 27, and that discussion is reiterated here.

With respect to *Merkel*, the Office Action states only that it "discloses providing zirconium tungstate," and makes the wildly conclusory and unsupported allegation that it would have been obvious to one of ordinary skill in the art "to modify the *Leibowitz/Mikagi* by providing zirconium tungstate, as taught by *Merkel*, for the purpose of providing greater range of negative coefficient of thermal expansion without yarns."

It is noted that like *Leibowitz* and *Mikagi*, *Merkel* is directed to subject matter wholly unrelated to zero insertion force contact pin sockets or their formation. This fact alone belies any suggestion that a person of ordinary skill in the *relevant* art would be motivated to make the proposed *Leibowitz/Mikagi/Merkel* combination. Furthermore, even if such combination were made, the result would be of no relevance to the present invention, as *none* of these references relates in any way to formation of zero insertion force sockets. Reconsideration and withdrawal of the § 103 rejection of claims 22, 23, and 27 is therefore requested.

Claim 30 was rejected under § 103 as being unpatentable over the proposed hypothetical combination of *Leibowitz* and *Mikagi*, further in view of "Official Notice." According to the Office Action, "it is well known in the art to form the second aperture smaller than the first aperture for the purpose of preventing a conductive material to [sic] escaping from the aperture during assembly."

It is submitted that the foregoing remarks with respect to the § 103 rejection of claims 18-19, 21, and 26 are equally applicable to the rejection of claim 30, and those remarks are reiterated here. With regard to the issue of which Official Notice is made, this is believed to be of no relevance, inasmuch as the proposed *Leibowitz/Mikagi* combination, even if made, would neither teach nor suggest a structure or method even remotely resembling the claimed invention. Reconsideration and withdrawal of the rejection of claim 30 is therefore requested.

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5. *The Remaining Claims.* The Office Action notes that no art rejection is applied to claims 29, 31-32, 34-36, 39-40 and 42-46 owing to "a great deal of confusion and uncertainty as to the proper interpretation" of the claims.

It is respectfully submitted that any ambiguity in the claims has been eliminated by way of the foregoing amendments to the claims, as discussed in Section 3 above, and that consequently there is no basis for rejecting the claims on this basis.

Though no art rejections were applied to these claims, Assignee takes this opportunity to reiterate the arguments made in Section 4 above with respect to the § 103 rejections, and respectfully submits that there is similarly no basis for rejecting these claims based on the cited prior art. There is utterly no basis for suggesting that a person of ordinary skill in the art would be motivated to make the hypothetical prior art combinations proposed in the Office Action. Moreover, even if the combinations were made, they could not possibly render the claims obvious, given the un-relatedness of the subject matter of each of the cited references to the invention disclosed and claimed in the present application.

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CONCLUSION

In view of the foregoing, it is believed that each of the claims pending in the application allowable, and that the application as a whole is in proper form and condition for allowance. Examination and allowance is therefore respectfully requested, such that the application may advance to issuance at the earliest possible date. If the Examiner believes that the application can be placed in even better condition for allowance, he is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: 8-FEB-03

ATTORNEY FOR ASSIGNEE

Hugh R. Kress
Hugh R. Kress
Reg. No. 36,574
WINSTEAD SECHREST & MINICK, P.C.
2400 Bank One Center
910 Travis Street
Houston, Texas 77002
(713) 650-2714(voice)
(713) 650-2400 (fax)

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APPENDIX A
"MARKED UP" VERSIONS OF AMENDED TEXT
PURSUANT TO 37 C.F.R. § 1.121

In the Claims

The claims were amended as follows:

① 8. (twice amended) A method of forming a socket for receiving a terminal pin from an electronic component therein, comprising [in order]:

(1) first forming a layer of a first material on an upper surface of a substrate;
(2) second forming a layer of a second material on said [said] layer of said first material;

and

(3) third forming an aperture in said first and second layers to expose said upper surface of said substrate;

wherein said first material has a positive coefficient of thermal expansion and said second material has a negative coefficient of thermal expansion.

② 19. The method in accordance with claim 18, further comprising, prior to step (1) of forming a layer of a first material:

forming an electrical contact pad on said substrate such that said contact pad is at least partially exposed within said aperture.

③ 21. The method in accordance with claim 18, wherein said first material is a polyimide.

④ 22. The method in accordance with claim 18, wherein said second material is zirconium tungstate.

⑤ 23. The method in accordance with claim 22, wherein said zirconium tungstate is single-crystal zirconium tungstate.

⑥ 26. The method in accordance with claim 18, further comprising, between step (1) of forming a layer of a first material and step (2) of forming a layer of a second material:

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applying an interfacial material between said layer of first material and said layer of second material to permit relative movement between said layer of first material and said layer of second material.

(1)

27. The method in accordance with claim 18, wherein said substrate is ceramic.

(2)

29. (twice amended) The method in accordance with claim 18, wherein said layer of first material is bonded to said substrate using a spin-on process followed by a [and] photo [define/etch] -define and -etch process.

(3)

30. The method in accordance with claim 18, wherein said step (3) of forming said aperture comprises forming a first aperture in said layer of first material and a second aperture in said layer of second material, wherein said second aperture has a linear dimension smaller than said first aperture.

(4)

31. (twice amended) A method of electrically connecting an electronic component having a contact pin extending therefrom to a contact pad on a substrate, comprising[, in order]:

- (1) first forming a layer of a first material on an upper surface of said substrate;
- (2) second forming a layer of a second material on said [said] layer of said first material; and
- (3) third forming an aperture in said first and second layers to expose said upper surface of said substrate;

wherein said first material has a positive coefficient of thermal expansion and said second material has a negative coefficient of thermal expansion;

and wherein said method further comprises[, in order, subsequent to step (3) of forming an aperture in said first and second layers]:

- (4) fourth heating said layer of first material and said layer of second material to a temperature substantially above a range of normal operating temperatures for said electronic component;
- (5) fifth inserting said contact pin into said aperture; and

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(6) sixth cooling said layer of first material and said layer of second material to a temperature within said range of normal operating temperatures for said electronic component.

(1) 32. The method in accordance with claim 31, further comprising, prior to step (1) of forming a layer of a first material:

forming an electrical contact pad on said substrate such that said contact pad is at least partially exposed within said aperture.

(12) 34. The method in accordance with claim 31, wherein said first material is a polyimide.

(13) 35. The method in accordance with claim 31, wherein said second material is zirconium tungstate.

(14) 36. The method in accordance with claim 35, wherein said zirconium tungstate is single-crystal zirconium tungstate.

(15) 39. The method in accordance with claim 31, further comprising, between step (1) of forming a layer of a first material and step (2) of forming a layer of a second material:

applying an interfacial material between said layer of first material and said layer of second material to permit relative movement between said layer of first material and said layer of second material.

(16) 40. The method in accordance with claim 31, wherein said substrate is ceramic.

(17) 42. The method in accordance with claim 31, wherein said layer of first material is bonded to said substrate using a spin-on and photo define/etch process.

(18) 43. The method in accordance with claim 31, wherein said step (3) of forming said aperture comprises forming a first aperture in said layer of first material and a second aperture in said layer of second material, wherein said second aperture has a linear dimension smaller than said first aperture.

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(W) 44. The method in accordance with claim 31, wherein said step (4) of heating said layer of first material and said layer of second material comprises heating said layer of first material and said layer of second material to a temperature of between approximately 200°C and 250°C.

(D) 45. The method in accordance with claim 44, wherein a normal operating temperature for said electronic component is approximately 100°C.

(N) 46. The method in accordance with claim 31, wherein said step (6) of cooling said layer of first material and said layer of second material comprises cooling said layer of first material at a rate slower than the rate at which said layer of second material is cooled.

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